Experimental Investigation on the Transient Switching Behavior of SiC MOSFETs Using a Stage-Wise Gate Driver

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***Abstract*—A multiple stage gate driver for SiC MOSFETs based on a switched resistor topology is introduced and a hardware realization is presented. The measurement setup is shown in detail to highlight the quality of the shown measurement results. The evaluation of the stage-wise driver is conducted by comparing the switch and diode peak voltages as well as peak currents with regard to the switching losses to a reference driver. The switching transients are generated using a double pulse test bench. A detailed investigation on two- and three-stage operation for both, the turn-on and turn-off events are presented. A variation of gate resistors and different timings is conducted for each stage and evaluated using the resulting measurements. It is shown that the drain-source peak voltage is reduced by 45% while maintaining equal turn-off losses. Analogously, a reduction of 51% of the diode peak voltage and a reduction of 50% of the peak reverse recovery current at the same time is feasible for equal turn-on losses.**

***Index Terms*—MOSFET switches, power electronics, semiconductor device measurements, switched resistor circuits, test equipment.**

I. Introduction

POWER electronic converters are used in a wide field of applications and a growing tendency is seen. Their appearance is growing in low- and medium-voltage applications. They are the key technology for renewable energies or electric traction systems, especially electric vehicles [1]-[3].

Reductions in volume and weight are a crucial aspect to achieve lower costs of the converters. This leads to a higher integration level of the converters [4], [5]. A high integration level creates the need for good thermal power flow by using e.g., thermal interface materials [6]. Furthermore, this integration level of power electronic converters can be increased using the emerging high-temperature wide-bandgap (WBG) power semiconductors [7]-[9] as higher switching frequencies can be achieved, which in turn allows a reduction of the filter size. However, higher switching frequencies and steeper switching slopes are the source for higher electromagnetic interference (EMI) [10].

An extensive comparison of the switching performance between insulated-gate bipolar transistors (IGBTs) and silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) is presented in [11], [12]. Considerable efforts have been made to affect the switching behavior of IGBTs, for example to influence the EMI, voltage stress or switching losses [13]-[16].

As the switching times of SiC MOSFETs are reduced by at least a decade compared to the switching times of IGBTs, the design of an active gate driver (AGD) is more challenging. Nevertheless, various approaches, which are widely known for silicon power semiconductors, are found in literature, such as protection circuitry [17], current controlled gate drivers [18], resonant gate drivers [19] or gate drivers for series connected MOSFETs [20] or medium-voltage SiC MOSFETs [21]. Some investigations tend to handle parasitic turn-on [22], [23] or influence the switching speed using passive components in the gate path [24]-[26]. Very high switching speeds for WBG power semiconductors are achieved using inductive feedback as shown in [27]. Similar to integrated current sense structures for IGBTs, integrated current sense structures of SiC MOSFETs are appearing for protection or current sensing applications [28].

A two-stage AGD using analog circuitry with high bandwidth is presented in [29]. A multi-level AGD influencing the gate voltage during the Miller plateau is shown in [30].

In this work, a multiple-stage AGD for a 1.2 kV SiC MOSFET *CPM2-1200-0040B* based on a switched resistor topology is presented. A similar approach as shown in [15], [30] is followed to influence the switching behavior. The influence on the switching behavior for two- and three-stage operation is shown for the turn-on as well as the turn-off event. The investigations are evaluated against a reference push-pull gate driver. The goal is to show that the voltage peaks and current peaks can be reduced individually without a penalty on switching losses. TABLE I lists the device pa-

TABLE I
Specifications of the SiC MOSFET and Test Setup

Description	Specifier	Value
Blocking voltage	U_{DSS}	1200 V
Rated current	I_D	63 A
DC-link voltage	U_{dc}	700 V
Test current	I_D	60 A
Junction temperature	ϑ_j	35 °C

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rameters and test conditions at which the investigations are carried out. The junction temperature ϑ_j is given as 35 °C as all measurements are conducted at room temperature inside the test bench. Due to the fast switching slopes of the SiC devices, high bandwidth equipment has to be used and the correct employment of the latter is crucial for accurate measurement results [31]. Therefore, a dedicated section dealing with the measurement setup is included in this paper.

II. Stage-Wise Gate Driver Topology

The proposed stage-wise driver consists of a state-of-the-art voltage source gate driver using a variable gate resistance R_{gate}. The influence on the switching behavior is accomplished by changing the value of the gate resistance during the switching action. The presented topology already led to good results using silicon IGBTs as shown in [15]. In comparison to a switching event using an IGBT, the fall and rise times of voltage and current of a SiC device are at least a decade faster. This means, that if the switching event of an IGBT lasts for 100 ns (e.g., see [15], Fig. 11), it will last for less than 10 ns when using a SiC device. The gate driver, which is presented in [15], has a minimum time resolution of 10 ns due to the limited clock speed of the field-programmable gate array (FPGA). A timing of less than 1 ns is required to be able to influence the switching behavior of SiC devices. The employed topology of the driver is shown in this section. The high resolution timing, which is required as input stage to the driver hardware, is introduced in section III.

A. Topology

The schematic topology of the driver is shown in Fig. 1. It consists of three parallel branches, of which each constitutes of a push-pull stage configuration. Each branch consists of a turn-on and turn-off gate resistance $R_{g,on,n}$, $R_{g,off,n}$, an n-channel and p-channel MOSFET $Q_{on,n}$, $Q_{off,n}$ as well as a dual low-side driver chip IC_n. A comparison among several commercial gate driver integrated circuits (ICs) and n- and p-channel MOSFETs is conducted. The ICs with the fastest rise times (n-channel) or fall times (p-channel) using a dummy 10 nF capacitive load are selected. The selected devices are listed in TABLE II including the rise and fall times using the 10% . . . 90% borders of the dummy and gate capacitor voltage. The gate-source capacitance C_{gs} of the selected power semiconductor is 2 nF [32]. Assuming a *RC* charging curve, the time constant is reduced by a factor of 5 for the given SiC MOSFET compared to the dummy capacitor, resulting in 1.9 ns. However, the rise and fall times are still significant compared to the envisaged time resolution and the expected duration of the switching events. As the aim of the stage-wise driver is to only partially charge (or discharge) the gate capacitance during each stage, only a fraction of the indicated rise/fall time is required and thus within an acceptable range for the presented driver. The gate driver is supplied using the supply voltages $U_{GS,off} = 0$ V and $U_{GS,on} = 18$ V.

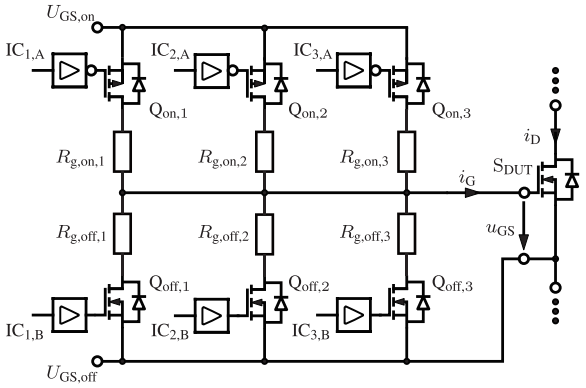


Fig. 1. Topology of the proposed stage-wise driver.

TABLE II
Selected Devices for the Driver Design

Device	Part nr.	rise/fall time	
IC_n	*UCC27523*		
$Q_{on,n}$	*BSZ180P03NS3E*	1.9 ns[1]	9.4 ns[2]
$Q_{off,n}$	*DMN3035LWN*	1.9 ns[1]	9.4 ns[2]

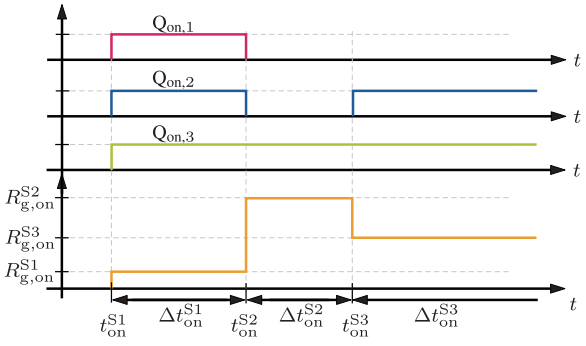


Fig. 2. Operation principle of the stage-wise driver.

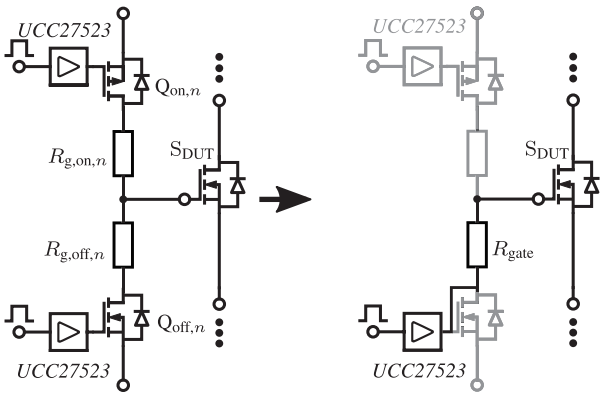
B. Operation Principle

The operation principle of the stage-wise driver is shown using an exemplary sequence for a turn-on event plotted in Fig. 2. During a state *S*, one or more MOSFETs $Q_{on,x}$ are turned on resulting in an effective gate resistance $R^S_{g,on}$. In the plotted exemplary waveforms, the switches $Q_{on,1}$, $Q_{on,2}$ and $Q_{on,3}$ are turned on at the same time during stage one. The effective first stage gate resistor results in

$$R^{S1}_{g,on} = R_{g,on,1} \parallel R_{g,on,2} \parallel R_{g,on,3}.$$

The first stage lasts for a time Δt^{S1}_{on}. Analogously, the gate resistance for the second stage is set to $R^{S2}_{g,on} = R_{g,on,3}$ for a duration Δt^{S2}_{on}. The third stage is, in this example, the last stage and thus lasts until the device under test (DUT) is switched off. This is indicated by setting the third stage tim-

[1] The indicated time is normalized to the gate capacitance $C_{gs} = 2$ nF.
[2] This is the measured rise/fall time using a 10 nF capacitance.



(a) Stage-wise driver. (b) Reference driver.

Fig. 3. Reference driver circuit.

ing to infinite $\Delta t_{\mathrm{on}}^{\mathrm{S3}} = \infty$.

C. Gate Driving Strategy

The goal of manipulating the switching waveforms is to achieve lowest switching losses while reducing the device stress at the same time. A similar approach as used in [15], [30] is employed.

This goal is achieved with an initial fast (dis)charging of the gate. Therefore, the smallest possible gate resistance is chosen for the first stage. However, a small gate resistance results in a high u_{DS} overshoot (turn-off event) or a high i_S, u_{Diode} overshoot (turn-on event), which are reduced by slowing down the (dis)charging process during the second stage using an increased gate resistance. A third stage, using a small gate resistance, is appended because the second stage resistance would result in very high switching losses for the remaining switching process.

However, besides the qualitative approach, no quantitative approach regarding timing and resistor values is known prior to the investigations. Therefore, a large variation of the different timings and resistor values are conducted to allow the deduction of an optimum driving strategy.

D. Reference Design

To allow an evaluation of the stage-wise gate driver, a classical single stage reference driver is needed. To avoid any unnecessary influence of, for example, the layout, on the switching behavior, the stage-wise driver is slightly modified, as shown in Fig. 3. One channel of the dual low side gate driver *UCC27523* is reconfigured to directly drive the gate resistance R_{gate}.

III. Hardware Realization

Parasitic inductances or capacitances have a high impact on the switching behavior [33]. Especially, when switching using high voltage or current slopes, the influence of these parasitic elements rises. Thus, a good layout of the switching cell and driver is crucial to achieve the desired results.

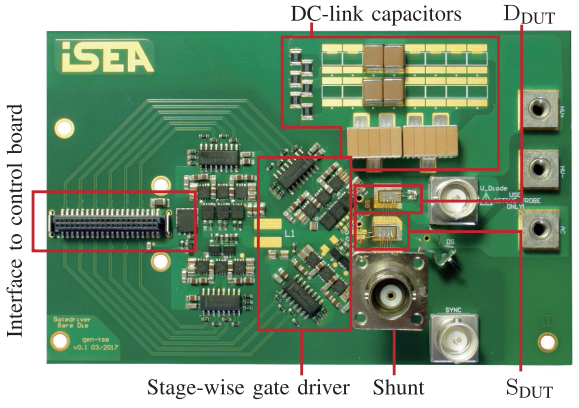


Fig. 4. Photograph of the PCB containing the driver and SiC bare dies.

TABLE III
Valuse of the Different Stary Inductances

Inductance	Value	Inductance	Value
$L_{\sigma,\mathrm{DC}}$	3.8 nH	$L_{\sigma,\mathrm{Switch}}$	2.0 nH
$L_{\sigma,\mathrm{Diode}}$	1.7 nH	$L_{\sigma,\mathrm{Shunt}}$	6.8 nH

Apart from the switching cell and driver board, the control board is introduced. The control board generates the different gate signals for the different branches.

A. Switching Cell and Driver Board

The printed circuit board (PCB) containing the switching cell and gate driver is pictured in Fig. 4. The control signals for the driver chips are transmitted using low-voltage differential signaling (LVDS) from the FPGA on the control board. A LVDS to single ended converter (*SN65LVDS048AD*) controls the dual low side driver ICs. The high-side gate is short circuited on the PCB (as seen in Fig. 4) as only the low-side MOSFET S_{DUT} is switched in the double pulse test. A close-up view on the low-side MOSFET is seen in Fig. 5. The Bayonet Neill-Concelman (BNC) plugs allow a repeatable measurement of the high-side diode voltage u_{Diode} and low-side drainsource voltage u_{DS}. The source current is measured using a T&M *SDN-414-10* current viewing resistor (CVR). The different stray inductances of the switching cell are determined using a current pulse generator [34] and methodology as described in [33]. The resulting values, corresponding to the schematic shown in Fig. 8, are listed in TABLE III. It is noticed, that the CVR is responsible for 47.5% of the total stray inductance.

B. Control Board

A photograph of the front and back side of the control board is shown in Fig. 6(a) and Fig. 6(b). The board hosts an *AT32UC3A1512* microcontroller (MCU) and a Xilinx Spartan 6 *XC6SLX9* FPGA. The MCU connects to a personal

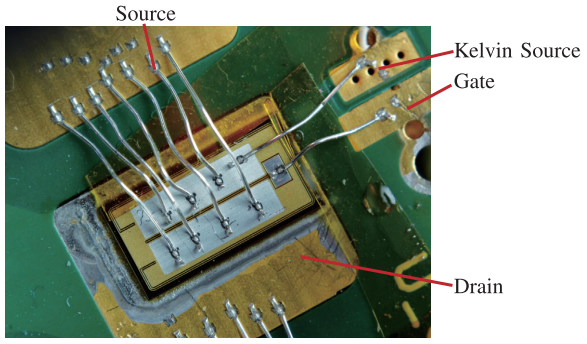
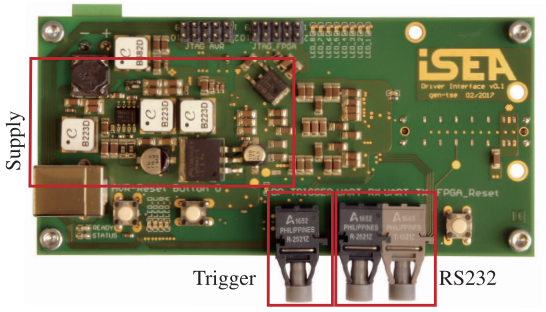
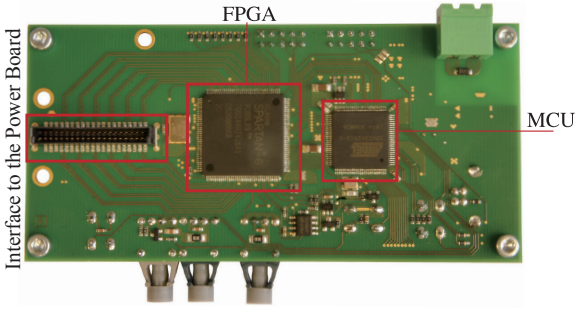


Fig. 5. Close-up view on the low-side SiC bare die.



(a) Top view



(b) Bottom view

Fig. 6. Photograph of the control board.

computer (PC) via *RS232* to allow on the fly configuration of the FPGA. A serial peripheral interface (SPI) bus ensures communication between the FPGA and MCU.

The main function of the FPGA is the generation of the different gate signals for each branch. A precise time resolution of less than 1 ns is required for an appropriate control of the SiC power semiconductors. The maximum clock speed of the employed FPGA of 300 MHz does not allow a higher time resolution than 3.33 ns. To achieve higher time resolutions, the delay-locked loop (DLL) functionality of the digital clock manager (DCM) of the FPGA is used. A very precise timing is achieved using the phase shift φ, as shown in Fig. 7. In total, four DCM blocks are available in the FPGA. Using a clock frequency of 50 MHz, the DLL allows a precise timing control of the edge of a signal of up to 23 ps.

IV. Measupement Setup

Measuring the voltage and current waveforms of SiC de-

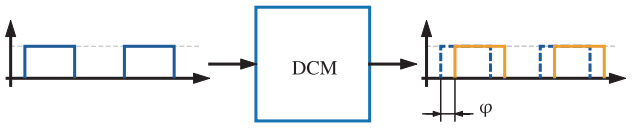


Fig. 7. Delay-locked loop operation principle.

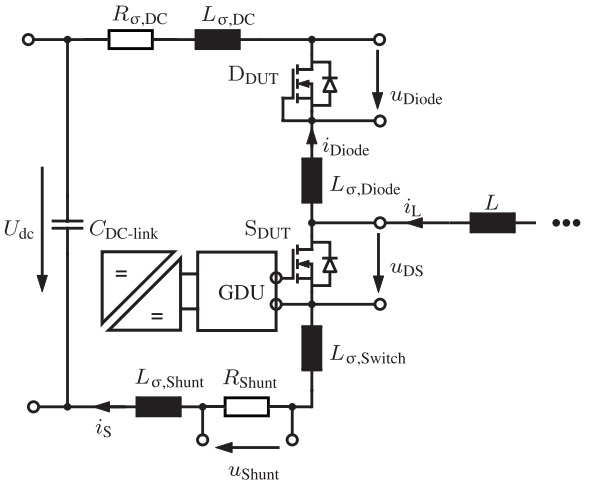


Fig. 8. Schematic of the switching cell used for the double pulse tests.

vices properly is not a trivial task [31]. As the measurement setup influences the resulting measurements to a large extend [35], a detailed description of the employed setup is shown prior to the main investigations on the gate driver.

The evaluation of the driver is made by comparing the resulting transient switching waveforms of the low-side semiconductor to the measurement results achieved using a push-pull reference driver. A double pulse test bench [36] is employed to conduct automated series measurements using different DC-link voltages, currents and temperatures [37].

The waveforms are recorded using a Teledyne LeCroy *HDO6104* oscilloscope using a vertical resolution of 12 bit, 1 GHz bandwidth and a 2.5 $^{GS}/_{s}$ sample rate. A schematic of the electrical circuit of the switching cell is shown in Fig. 8. Two 900 V, 1.25 µF CeraLink capacitors are used in parallel with four ceramic capacitances to form the DC-link capacitor $C_{DC\text{-}link}$. The voltage measurements u_{DS}, u_{Diode} and u_{GS} are made between the drain tab and kelvin source contacts. The low-side switch current i_S is measured using the indicated CVR.

The high-side diode current i_{Diode} is calculated using the low-side current i_S and inductor current i_L using (1). As the inductor current is not measured during the double pulse test, it is retrieved using a linear interpolation of the switch current i_S prior to turning the switch off at the time where it is still fully on ($t = t_{turn\text{-}off,-}$) and shortly after it is switched back on ($t = t_{turn\text{-}on,+}$) as indicated in (2) and (3).

$$i_{Diode} = i_L - i_S \tag{1}$$

$$i_L\,(t = t_{turn\text{-}off}) = i_S\,(t = t_{turn\text{-}off,-}) \tag{2}$$

$$i_{\mathrm{L}}\left(t = t_{\text{turn-on}}\right) = i_{\mathrm{S}}\left(t = t_{\text{turn-on,+}}\right) \tag{3}$$

A certain inaccuracy in the given current measurement method is taken into account. First, the measured source current i_{S} does not exactly represent the MOSFET channel current due to the parasitic output capacitance C_{oss}. However, literature shows that the influence of the output capacitance C_{oss} cancel each other when considering the sum of the turn-on and turn-off losses [38]. Besides calorimetric switching loss measurements, no accurate MOSFET channel current measurement technique, which is independent of the output capacitance C_{oss}, is known. For precisely this reason, the later on conducted measurements are compared to reference measurements which are recorded under exactly the same conditions. Second, the high-side diode current i_{Diode} is, besides the output capacitance C_{oss} of the high-side switch, additionally distorted by parasitic capacitances across the load inductance, or generally between the AC terminal and ground. The latter could be improved by using a CVR in the high-side path in combination with isolated low voltage measurement equipment.

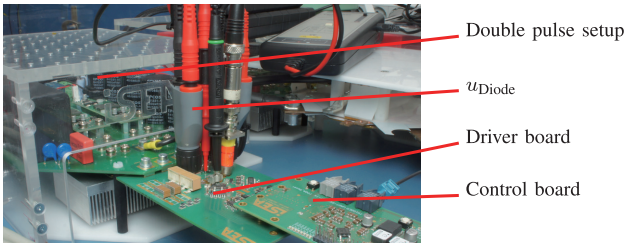
As the CVR connects the oscilloscope ground to the source potential of the low-side switch, the utilization of a further passive probe is not envisaged as the grounding terminal of the probe would create a ground loop via the oscilloscope to the CVR. This would facilitate circulating currents through the shielding of the coaxial cables and herewith disturb the measurements [35]. However, as an extensive study between various active differential and passive probes for small and large signal measurements got conducted prior to this work, the passive probe *PP018-2* largely outperforms the remaining probes for gate voltage measurements.

Thus, the following compromise is made: Exactly the same double pulse measurement is conducted twice after each other, first with only the passive probe connected to gate followed by a measurement with only the coaxial cable of the CVR connected. The gate voltage is measured additionally using the active probe for both measurements, which is used to synchronize and merge both measurements. The use of the active probe signal to merge the merging procedure is considered as valid, as the repeatability of the measured signal is very good. Using this procedure, it is guaranteed that no unnecessary distortion occurs due to circulating currents in the coaxial shielding. The only drawback, which is disregarded, is the influence of an eventual jitter of the various ICs used for the AGD. The employed measurement probes are summarized in TABLE IV. A photograph of the setup is pictured in Fig. 9.

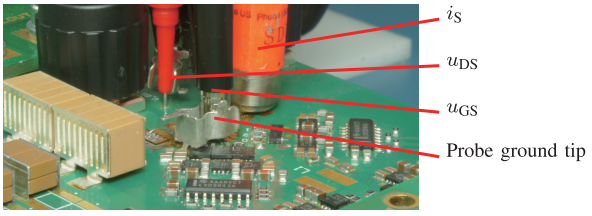
As the switching times of the SiC MOSFETs, which are within 10 ns ... 20 ns, are in the same range as the probedelays, a delay compensation is required. As no appropriate information is available in the provided data sheets, the individual propagation delays of the probes are measured using a Tektronix *Type 109* pulse generator and a high-voltage probe calibrator *KHT 1000*. The resulting values are indicated in TABLE IV. The propagation delay of the CVR is due to the coaxial cable (*Radiall R284C0351005*) with a length of 1 m and external 50 Ω terminator.

TABLE IV
MEASUREMENT EQUIPMENT

Manufacturer	Part Nr.	Measured signal	Probe delay	Bandwidth
PMK	*BumbleBee*	u_{DS}, u_{Diode}	12.3 ns	300 MHz
Testec	*TT-SI 9101*	u_{GS}	11.7 ns	100 MHz
Teledyne LeCroy	*PP018-2*	u_{GS}	6.3 ns	500 MHz
T&M Research	*SDN-414-10*	i_{S}	5.4 ns	2000 MHz



(a) Measurement setup



(b) Close up view

Fig. 9. Photograph of the measurement setup.

V. REFERENCE MEASUREMENTS

The measurements using the reference driver are introduced and presented in this section. As the stage-wise gate driver makes use of various gate resistances during a single switching event, the results cannot be simply compared to a reference measurement using a specific gate resistance. Thus, the reference measurements are made using various gate resistances in the range $R_{\mathrm{gate}} = 0.5\ \Omega \ldots 10\ \Omega$.

A. Measurements of the Turn-On Event

The turn-on measurements cover the turn-on event of the low-side switch as well as the turn-off event of the high-side diode. The measured waveforms using the different gate resistors are shown in Fig. 10. The respective voltage and current slopes are indicated for the current waveforms as well as for the switch and diode drain-source voltage u_{DS}, u_{Diode}. The voltage and current fall and rise slopes are indicated in the respective figures. The slopes are calculated using the 10% ... 90% borders of the waveforms, excluding the inductive voltage drop during the turn-on event (see Fig. 10). Depending on the gate resistance R_{gate}, current slopes ranging from $3.4\ {}^{\mathrm{A}}/_{\mathrm{ns}} \ldots 20\ {}^{\mathrm{A}}/_{\mathrm{ns}}$ are reached. The slope of the low-side drain-source voltage $\frac{\mathrm{d}u_{\mathrm{DS}}}{\mathrm{d}t}$ reaches values from $-19\ {}^{\mathrm{V}}/_{\mathrm{ns}} \ldots -57\ {}^{\mathrm{A}}/_{\mathrm{ns}}$

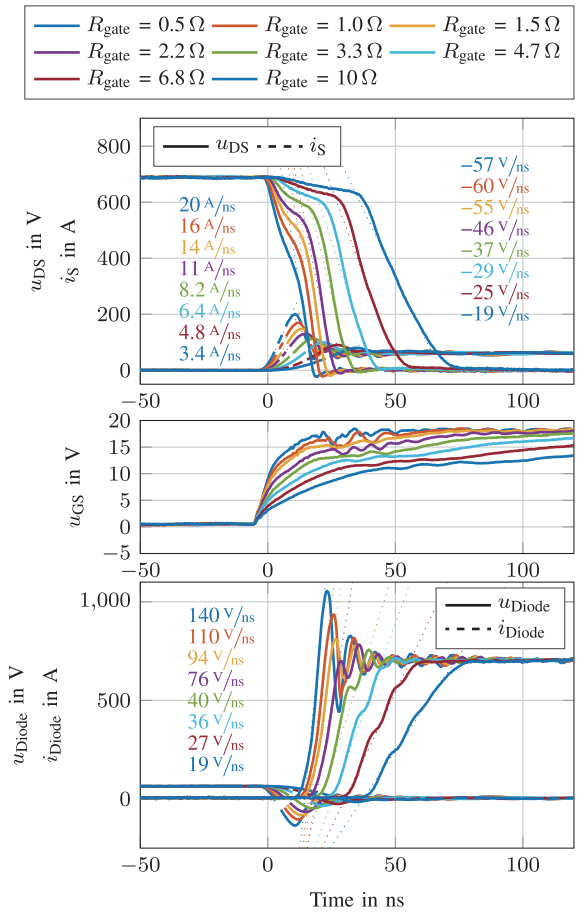


Fig. 10. Reference turn-on event measurements using different gate resistors.

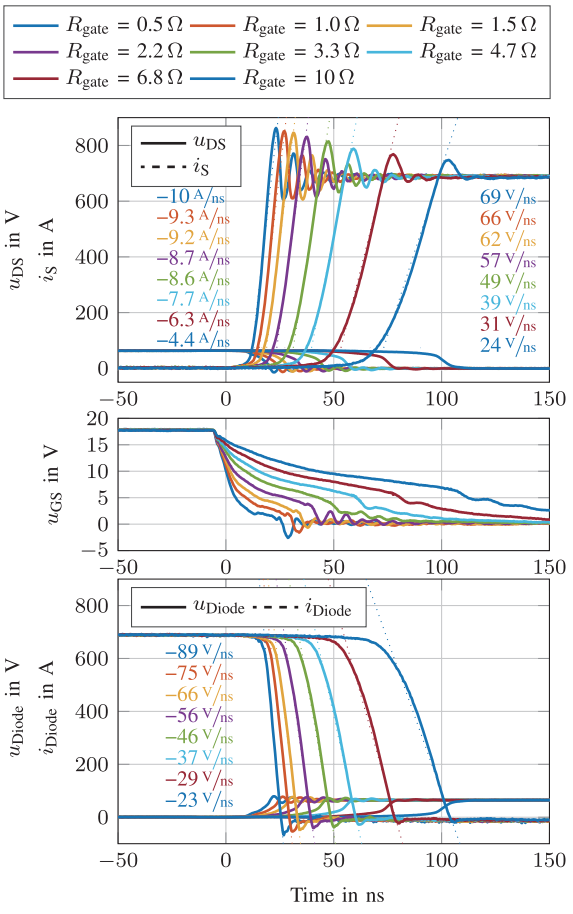


Fig. 11. Reference turn-off event measurements using different gate resistors.

whereas the voltage slope of the diode reach higher values ranging from 19 $^{A}/_{ns}$ ... 140 $^{A}/_{ns}$.

B. Measurements of the Turn-Off Event

Analogously, the reference measurements of the turn-off event are shown in Fig. 11 together with their corresponding slopes. The current slopes reach from −4.4 $^{A}/_{ns}$ ... −10 $^{A}/_{ns}$. The slope of the diode voltage u_{Diode} ranges from 22 $^{V}/_{ns}$ ... 82 $^{V}/_{ns}$ whereas the switch voltage slope $\frac{du_{DS}}{dt}$ ranges from −23 $^{V}/_{ns}$ ... −89 $^{V}/_{ns}$.

C. Switching Losses

The switching losses of the various switching transitions are calculated using

$$E_{sw} = \int_{t_{start}}^{t_{end}} p_{sw} dt = \int_{t_{start}}^{t_{end}} (u_{DS} \cdot i_S)\, dt.$$

The start and end times t_{start} and t_{end} are chosen using the 3% borders of the peak power. A more detailed description of the switching loss extraction algorithm is given in [15]. The resulting switching losses using the reference driver with various gate resistances are shown in Fig. 12.

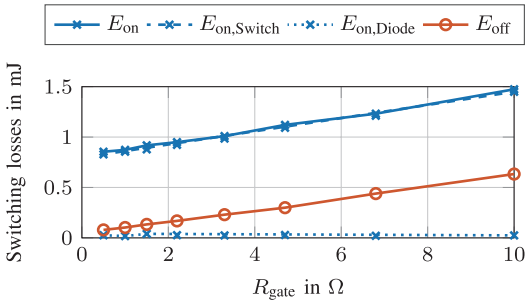


Fig. 12. Calculated switching losses using the reference driver with various gate resistances at U_{dc} = 700 V, I_D = 60 A.

VI. Stage-Wise Driver Turn-On Operation

The influence of the stage-wise gate driver on the turn-on event is investigated in this section. At first, a simple change of resistor, from a small value to a larger value, is shown. The aim of slowing down the gate charging is to reduce the diode peak voltage $\hat{U}_{Diode}$ and the switch peak current $\hat{I}_S$. Afterwards, a third stage is introduced, which further improves the switching behavior.

A. Investigations on the Two-Stage Turn-On Event

The two-stage turn-on event is investigated using the setup

TABLE V
TWO-STAGE DRIVER SETUP FOR THE TURN-ON EVENT

Stage S	$R^S_{\mathrm{g,on}}$	Δt^S_{on}
1	0.5 Ω	0 ns … 1.2 ns, ∞
2	2.2 Ω … 10 Ω	∞

TABLE VI
THREE-STAGE DRIVER SETUP OF THE TURN-ON EVENT

Stage S	$R^S_{\mathrm{g,on}}$	Δt^S_{on}
1	0.5 Ω	0.86 ns
2	50 Ω	0 ns … 15 ns
3	2.2 Ω	∞

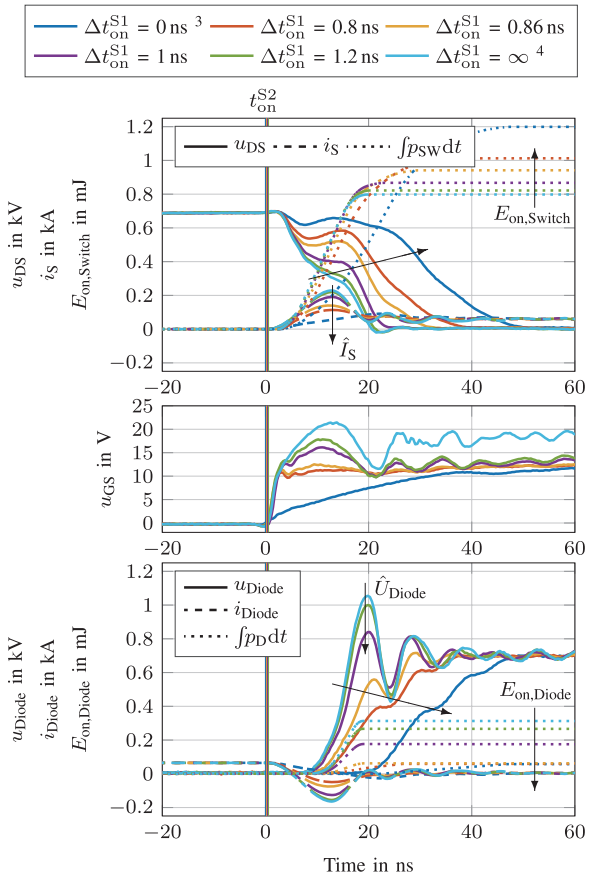


Fig. 13. Two-stage turn-on event waveforms using $R^{\mathrm{S2}}_{\mathrm{g,on}} = 10\ \Omega$.

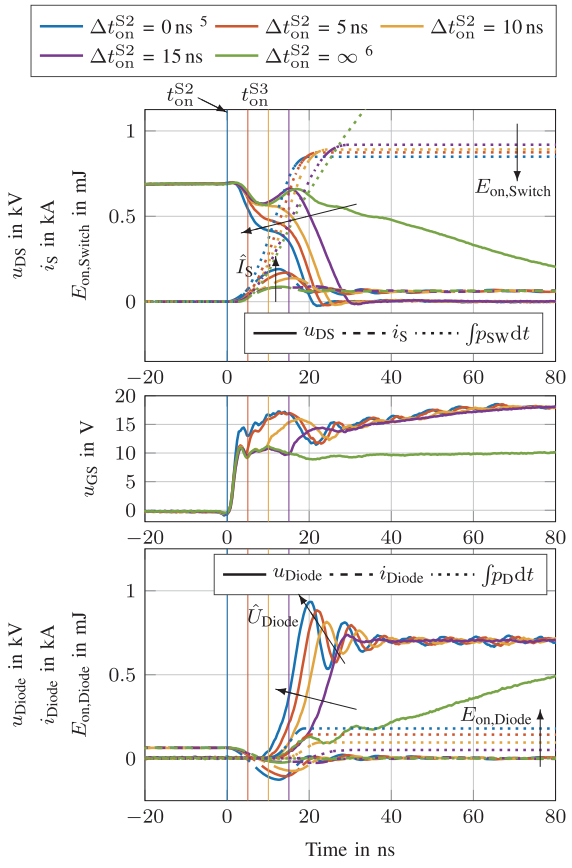


Fig. 14. Three-stage turn-on event waveforms.

as listed in TABLE V. The resulting transient waveforms using a second stage gate resistance $R^{\mathrm{S2}}_{\mathrm{g,on}} = 10\ \Omega$ are plotted in Fig. 13 including two reference waveforms ($\Delta t^{\mathrm{S1}}_{\mathrm{on}} = 0$ ns, $\Delta t^{\mathrm{S1}}_{\mathrm{on}} = \infty$) for comparison. It is seen, that it is possible to manipulate the waveforms between the two reference measurements. It is shown in Fig. 13, that the diode peak voltage $\hat{U}_{\mathrm{Diode}}$ is reduced down to the DC-link voltage U_{dc}, thus eliminating the overshoot. As it is seen from Fig. 13, that although the turn-on losses are increasing as expected with a shorter duration of the first stage, the losses in the diode are decreasing. As the total turn-on losses include the losses in the diode as well as the switch, an optimum operation point for the turn-on event using a two-stage gate driver has to be found.

B. Investigations on the Three-Stage Turn-On Event

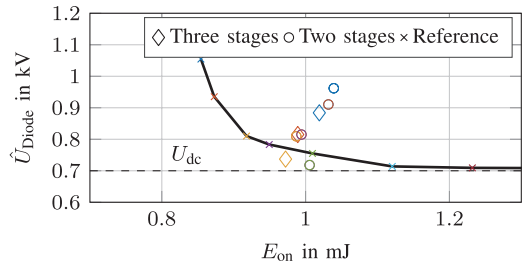
To improve the two-stage switching behavior, a third stage using a small gate resistance comparing to the second stage gate resistance $R^{\mathrm{S3}}_{\mathrm{g,on}} < R^{\mathrm{S2}}_{\mathrm{g,on}}$ is appended. The driver setup listed in TABLE VI is applied. A good initial setup is chosen for the first and second stage. The resulting waveforms are plotted in Fig. 14.

It is observed that, by introducing a third stage with a small gate resistance, the losses in the switch decrease comparing to the two-stage operation ($\Delta t^{\mathrm{S2}}_{\mathrm{on}} = \infty$). However, the diode losses as well as the device stress ($\hat{I}_{\mathrm{S}}$, $\hat{U}_{\mathrm{Diode}}$) increase at the same time. The evaluation of the performance of the three-stage operation is shown in the following section.

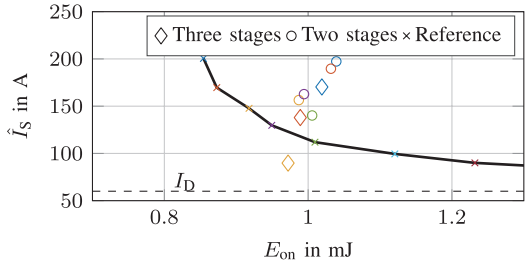
C. Evaluation of the Stage-Wise Turn-On Operation

The preceding sections showed the ability of the AGD to influence the stress and the switching losses of the power semiconductor. It becomes clear from Fig. 13, that during the

[3] Equivalents a single-stage turn-on event using $R_{\mathrm{gate}} = 10\ \Omega$.
[4] Equivalents a single-stage turn-on event using $R_{\mathrm{gate}} = 0.5\ \Omega$.
[5] Equivalents a two-stage turn-on event: $R^{\mathrm{S1}}_{\mathrm{g,on}} = 0.5\ \Omega$ to $R^{\mathrm{S2}}_{\mathrm{g,on}} = 2.2\ \Omega$.
[6] Equivalents a two-stage turn-on event: $R^{\mathrm{S1}}_{\mathrm{g,on}} = 0.5\ \Omega$ to $R^{\mathrm{S2}}_{\mathrm{g,on}} = 50\ \Omega$.



(a) High-side diode overshoot voltage vs. turn-on energy



(b) Reverse recovery peak current vs. turn-on energy

Fig. 15. Device stress vs. turn-on energy.

TABLE VII
TWO-STAGE DRIVER SETUP OF THE TURN-OFF EVENT

Stage S	$R^S_{\text{g,off}}$	Δt^S_{off}
1	0.5 Ω	12 ns … 16 ns
2	4.7 Ω, 12 Ω, 15 Ω, 18 Ω	∞

first stage, a high precision in the timing is required as very little influence (<1 ns) has a high impact on the remaining switching transient of the power semiconductor.

A quantitative comparison of the stress and the switching energy for the turn-on event is plotted in Fig. 15, containing both, the reference as well as the two- and three-stage measurements. It is seen, that using the two-stage operation, the device stress can be influenced over a wide range, however with additional costs in turn-on losses. A good two-stage parameter selection as a basis for the three-stage operation allows a reduction of the stress and of the losses at the same time, compared to the reference driver. A reduction of the diode peak voltage $\hat{U}_{\text{Diode}}$ by 51% as well as a reduction of the reverse recovery peak current $\hat{I}_{\text{S}}$ by 50% is reached for equal turn-on losses E_{on}.

VII. STAGE-WISE DRIVER TUREN-OFF OPERATION

Analogously to the turn-on event investigations, the influence of the different stages on the turn-off event is investigated. The impact of the two-stage operation on the switching transients is shown first, followed by an investigation of a third stage.

A. Investigations on the Two-Stage Turn-Off Event

The two-stage analysis is carried out using the driver setup

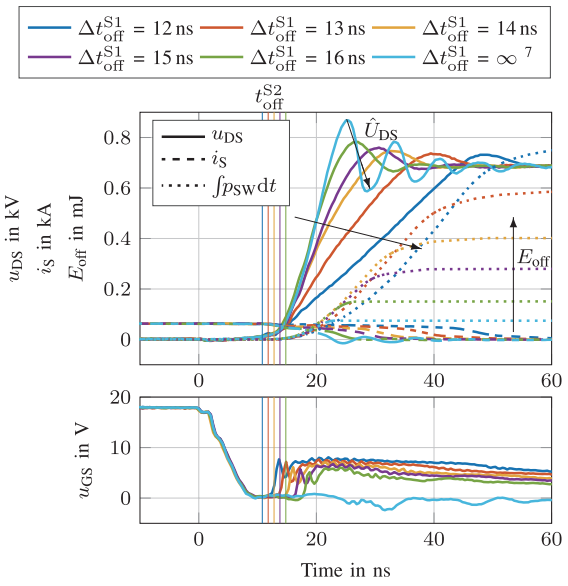


Fig. 16. Two-stage turn-off event waveforms using $R^{\text{S2}}_{\text{g,off}} = 15\ \Omega$.

TABLE VIII
THREE-STAGE DRIVER SETUP OF THE TURN-OFF EVENT

Stage S	$R^S_{\text{g,off}}$	Δt^S_{off}
1	0.5 Ω	15.6 ns
2	100 Ω	5 ns … 15 ns
3	4.7 Ω	∞

as shown in TABLE VII. The gate is discharged using a high current in the beginning and is slowed down after a certain time $\Delta t^{\text{S1}}_{\text{off}}$ with switching to a higher gate resistance $R^{\text{S2}}_{\text{g,off}}$.

The resulting waveforms are plotted in Fig. 16. The two-stage operation allows a reduction of the drainsource voltage peak $\hat{U}_{\text{DS}}$, however with increased turn-off losses.

B. Investigations on the Three-Stage Turn-Off Event

The influence of a third stage is shown using the setup listed in TABLE VIII. The time $\Delta t^{\text{S2}}_{\text{off}}$ is increased using a 2.5 ns step size. Fig. 17 shows the resulting waveforms. A slight increase of the peak voltage $\hat{U}_{\text{DS}}$ together with a reduction of the turn-off losses is observed. The rate of change of both quantities compared to the two-stage operation decides whether an overall improvement is achieved. It is noticed, that a noticeable effect on the waveforms is seen only a certain time after the gate resistance got changed.

C. Evaluation of the Stage-Wise Turn-Off Operation

It is shown, that an influence on the switching transients is as well possible during the turn-off event. However, certain delays in the reaction of the transient behavior are seen, as for example in the gate voltage waveform plotted in Fig. 16.

The resulting device stress ($\hat{U}_{\text{DS}}$), extracted from the two

[7] Equivalents a single-stage turn-off event using $R_{\text{gate}} = 0.5\ \Omega$.

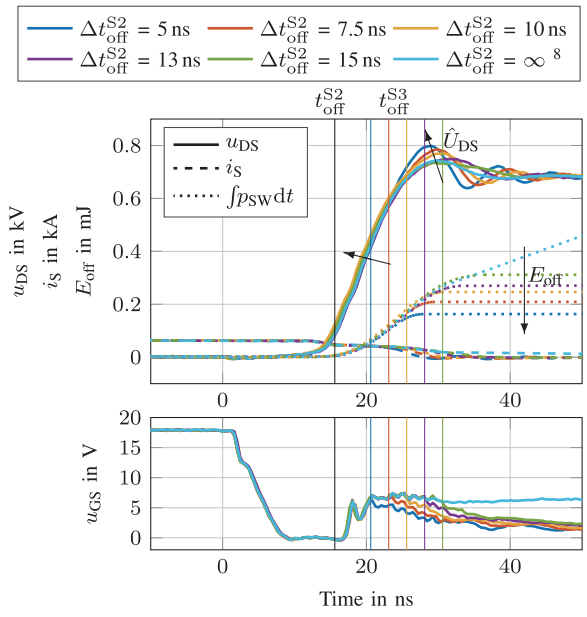


Fig. 17. Three-stage turn-off event waveforms.

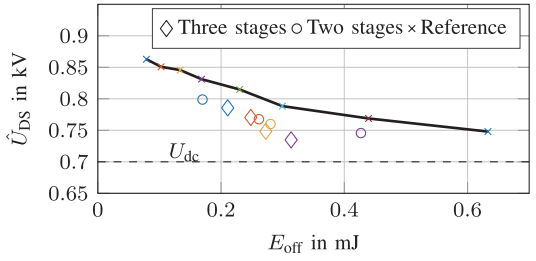


Fig. 18. Low-side switch voltage overshoot vs. turn-off energy.

and three-stage measurements, is plotted against the turn-off energy in Fig. 18. It is seen, that implementing a second stage during the turn-off event gives a better performance of the power semiconductor as all measurement points are found below the reference measurements. The introduction of a third stage shows the possibility of further improvement compared to the two-stage operation.

However, the key statement of the investigation is, that the introduction of an initial fast discharging stage is crucial to achieve improved switching behavior. All together, the drain-source peak voltage $\hat{U}_{\text{DS}}$ is reduced by up to 45% while maintaining equal turn-off losses E_{off}.

VIII. Summary of the Switching Behavior

A summary of the switching behavior using the variations of timing and resistances of the different stages is given for both, the turn-on as well as for the turn-off event of the SiC MOSFET. TABLE IX shows the influence of rising gate resistance $R_{\text{g,on}}^{S}$ and rising stage time Δt_{on}^{S} on the device stress, $\hat{I}_{\text{S}}$ and $\hat{U}_{\text{Diode}}$, as well as on the turn-on loss energies

[8] Equivalents a two-stage turn-off event changing from $R_{\text{g,off}}^{\text{S2}} = 0.5\ \Omega$ to $R_{\text{g,off}}^{\text{S3}} = 100\ \Omega$.

TABLE IX
Summary of the SiC MOSFET Turn-On Behavior

	$\hat{I}_{\text{S}}$	$\hat{U}_{\text{Diode}}$	$E_{\text{on,Switch}}$	$E_{\text{on,Diode}}$	E_{on}	Reference
$R_{\text{g,on}}^{\text{S1}}\uparrow$	↘	↘	↗	→	↗	Fig. 12, Fig. 15
$\Delta t_{\text{on}}^{\text{S1}}\uparrow$	↗	↗	↘	↗	↘	Fig. 13
$R_{\text{g,on}}^{\text{S2}}\uparrow$	↘	↘	↗	↘	↗	Fig. 13, Fig. 15
$\Delta t_{\text{on}}^{\text{S2}}\uparrow$	↘	↘	↗	↘	↗	Fig. 14
$R_{\text{g,on}}^{\text{S3}}\uparrow$	-	-	↗	↗	↗	

TABLE X
Summary of the SiC MOSFET Turn-Off Behavior

	$\hat{U}_{\text{DS}}$	E_{off}	Reference
$R_{\text{g,off}}^{\text{S1}}\uparrow$	↘	↗	Fig. 12, Fig. 18
$\Delta t_{\text{off}}^{\text{S1}}\uparrow$	↗	↘	Fig. 16
$R_{\text{g,off}}^{\text{S2}}\uparrow$	↘	↗	Fig. 18
$\Delta t_{\text{off}}^{\text{S2}}\uparrow$	↘	↗	Fig. 17
$R_{\text{g,off}}^{\text{S3}}\uparrow$	-	↗	

$E_{\text{on,Switch}}$ and $E_{\text{on,Diode}}$. Analogously, the influence of the gate resistances $R_{\text{g,off}}^{S}$ and timings $\Delta t_{\text{off}}^{S}$ on the transient voltage overshoot $\hat{U}_{\text{DS}}$ and turn-off energy E_{off} is tabulated in TABLE X.

The mechanism contributing to the performance improvement of the AGD, compared to the reference driver, relies on the modulation of the gate charge during the switching transient. A fast dis-/charging of the gate is envisaged during the switching phase, where the stress on the device is not critical. However, during the critical phases, the gate dis-/charging is reduced and the measurements show, that this results in less stress on the power semiconductor compared to a single-stage gate driver.

IX. Conclusions

In this work, a stage-wise gate driver based on a switched resistor topology for SiC MOSFETs has been presented. A detailed description of the measurement setup as well as the switching loss extraction has been shown as this is crucial to achieve reliable measurement results. The performance of the stage-wise gate driver was evaluated by benchmarking the device stress, resulting from the switching transients, against the switching losses. Furthermore, the evaluation included a comparison to a reference gate driver, based on a standard push-pull stage using various different gate resistances. A detailed analysis of the two- and three-stage operation of the AGD was conducted for the turn-on and the turn-off event.

It has been shown that the drain-source peak voltage $\hat{U}_{\text{DS}}$ got reduced by 45% while maintaining equal turn-off losses E_{off}. The turn-on event shows a reduction of 51% of the diode peak voltage $\hat{U}_{\text{Diode}}$ and a reduction of 50% of the peak reverse recovery current $\hat{I}_{\text{S}}$ at the same time for equal turn-

on losses E_{on}. This allows the utilization of a higher DC-link voltage, resulting in a higher power rating of a given converter with a given power semiconductor. This is crucial to reduce price per kilowatt of future high density power electronic converters.

The mentioned achievements should not be considered as the total potential of the driver as no optimization or search for an optimum point was carried out. Furthermore, it is noticed that a closed loop control of the switching trajectory is hardly achievable due to the large delays and late reaction of the power semiconductor.

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